NOV 2 1 2004 E

Tru

Docket No.: N0029.1650

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Shinichi Miyazaki et al.

Application No.: 10/771,451

Confirmation No.: 3851

Filed: February 5, 2004

Art Unit: 2812

For: METHOD OF FORMING A

Examiner: L. A. Gurley

CONNECTING CONDUCTOR AND

WIRINGS OF A SEMICONDUCTOR CHIP

RESPONSE TO RESTRICTION REQUIREMENT

U.S. Patent and Trademark Office 220 20th Street S. Customer Window, Mail Stop Amendment Crystal Plaza Two, Lobby, Room 1B03 Arlington, VA 22202

Dear Sir:

In response to the restriction requirement set forth in the Office Action mailed October 26, 2004 (Paper No. 1004).

The Examiner has required restriction between:

Group I: Claims 1-12, drawn to a method of making a semiconductor device, classified in class 438, subclass 618; and

Group II: Claims 13-18, drawn to a semiconductor device, classified in class 257, subclass 734+.

Application No.: 10/771,451 Docket No.: N0029.1650

Applicants hereby provisionally elect the Group I claims, claims 1-12, for continued examination without traverse. Applicant reserves the right to file a divisional application directed to the subject matter of the non-elected claims.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below. Consideration and allowance of the application is respectfully solicited.

Dated: November 24, 2004

Respectfully submitted,

Ian K Rlum

Registration No.: 42,336

DICKSTEIN SHAPIRO MORIN &

OSHINSKY LLP

1177 Avenue of the Americas

New York, New York 10036-2714

(212) 835-1400

Attorneys for Applicant

IRB/mgs

1.